IN THE CLAIMS:

Please amend the claims to read as the following:

Claim 1 (Currently Amended): A timing adjusting apparatus comprising:

an AD converter for receiving an input signal of which input signal level is converted into a digital signal to generate a digitized input signal; [[and]]

a counter circuit to which the digitized input signal, a counter clock signal and a trigger signal are provided so as to set a count number based on the digitized input signal and start counting the counter clock signal in response to the trigger signal, wherein an output signal is generated from the counter circuit at the timing of the counter clock signal reaching the count number; and

a binary-coded N-bit output counter for outputting the counter clock signal by counting an input clock signal and carrying out a count operation repeatedly, said counter clock signal being selected from one of N-bit output signals in accordance with a rotation of a disk.

Claim 2 (Original): The timing adjusting apparatus according to claim 1, wherein the digitized input signal is set as the count number when the trigger signal is input.

Claim 3 (Canceled).

Claim 4 (Canceled).

Claim 5 (Previously Presented): The timing adjusting apparatus according to claim 1, wherein said input signal is determined by an adjusting time which delays an output timing of the output signal with regard to the trigger signal.

Claim 6 (Previously Presented): The timing adjusting apparatus according to claim 1, wherein said counter clock signal is supplied to the counter circuit continuously irrespective of timings of the digitized input signal or the trigger signal being supplied thereto.

Claim 7 (Canceled).